IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	
Robert Sheffield et al.	Group Art Unit: 1753
Appln. No.: 10/667,491	Examiner: Luan V. Van
Filed: September 23, 2003	Confirmation No.: 1242
For: REDUCED CIRCUIT TRACE ROUGHNESS FOR IMPROVED SIGNAL PERFORMANCE	Customer No.: 21967

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REPLY BRIEF

Sir:

This Reply Brief is submitted in response to the Examiner's Answer dated October 31, 2006.

ARGUMENT

The Examiner's Answer dated October 31, 2006, has been received and carefully considered. Applicants appreciate the withdrawal of the rejections of claims 1-6, 19 and 20 in the Examiner's Answer based on Taylor et al. (U.S. Patent No. 6,309,528), Ozeki et al. (U.S. Patent Application No. 2002/0060090), Nagai et al. (U.S. Patent Application No. 2002/0155021), Taylor et al. (U.S. Patent No. 6,558,231), and

Lin et al. (U.S. Patent No. 5,273,938). However, the rejection of claims 1-6, 19 and 20 based on Tanaka et al. (U.S. Patent No. 4,959,507) remains.

In the Examiner's Answer, the Examiner asserts that, regarding claim 1, Tanaka et al. inherently discloses reducing a surface roughness of at least one surface of the conductive circuit trace on the surface of the circuit board layer so as to improve performance of a signal transmitted via the conductive circuit trace, as claimed. However, as stated in MPEP § 2112, "[i]n relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original). Also "[b]efore a reference can be found to disclose a feature by virtue of its inherency, one of ordinary skill in the art viewing the reference must understand that the unmentioned feature at issue is necessarily present in the reference." SGS-Thompson Microelectronics, Inc. v. International Rectifier Corp., 32 USPQ2d 1496, 1503 (Fed. Cir.) (unpublished), cert. denied, 115 S. Ct. 655 (1994) (emphasis added). Further "[a]n accidental or unwitting duplication of an invention cannot constitute an

anticipation." In re Marshall, 198 USPQ 344, 346 (C.C.P.A. 1978) (emphasis added).

As acknowledged by the Examiner, Tanaka et al. does not explicitly disclose reducing a surface roughness of at least one surface of the conductive circuit trace on the surface of the circuit board layer so as to improve performance of a signal transmitted via the conductive circuit trace, as claimed. Instead, as also acknowledged by the Examiner, Tanaka et al. teaches a method for forming a bonded ceramic-metal composite substrate so as to improve heat transmissivity between the copper circuit sheet and an electronic component (e.g., see from column 3, line 64, to column 4, line 13). Clearly, the teaching of Tanaka et al. differs from the claimed invention as set forth in claim 1. Thus, the allegedly inherent characteristic (i.e., improving transmitted signal performance) does not necessarily flow from the teachings of Tanaka et al., and no one of ordinary skill in the art viewing Tanaka et al. would have a reason to realize and therefore understand that the unmentioned feature at issue (i.e., improving transmitted signal performance) is necessarily present in Tanaka et al. Further, any duplication of the claimed invention by Tanaka et al. would merely be accidental or unwitting, and thus cannot constitute an anticipation by Tanaka et al.

Also, Tanaka et al. teaches polishing a copper circuit sheet so as to improve heat transmissivity between the copper circuit sheet and an electronic component (e.g., see from column 3, line 64, to column 4, line 13). Indeed, Tanaka et al. even teaches that polishing is only required where an electronic component is to be mounted to a copper circuit sheet so as to improve heat transmissivity therebetween, and that polishing is not required where the electronic component is electrically connected to copper circuit sheet, which would be where signals are transmitted (e.g., see from column 1, line 67, to column 2, line 7; column 3, lines 1-8). Such a teaching by Tanaka et al. is not even analogous to the claimed invention as set forth in claim 1. Thus, the allegedly inherent characteristic (i.e., improving transmitted signal performance) does not necessarily flow from the teachings of Tanaka et al., and no one of ordinary skill in the art viewing Tanaka et al. would have a reason to realize and therefore understand that the unmentioned feature at issue (i.e., improving transmitted signal performance) is necessarily present in Tanaka et al. Further, any duplication of the claimed invention by Tanaka et al. would merely be accidental or unwitting, and thus cannot constitute an anticipation by Tanaka et al.

In view of the foregoing, it is respectfully submitted that Tanaka et al. fails to teach, or even suggest, the claimed invention as set forth in claim 1. Thus, is it further respectfully submitted that claim 1 is allowable over Tanaka et al.

Claims 2-6, 19, and 20 are dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above, claims 2-6, 19, and 20 should also be allowable at least by virtue of their dependency on independent claim 1. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination. For example, claim 2 recites reducing the surface roughness by electropolishing the at least one surface, electrochemical polishing the at least one surface, electroplating the at least one surface, or vacuum depositing conductive material on the at least one surface. Tanaka et al. fails to disclose any of these claimed techniques. Also, claims 3-5 recite that the surface roughness of the at least one surface is reduced to no more than 20 microinches root-mean-squared (RMS), 10 microinches root-mean-squared (RMS), or 5 microinches root-mean-squared (RMS). The Examiner asserts that Tanaka et al. teaches such surface roughnesses by disclosing a mounting area median surface roughness no greater

than 3 μm and a mounting area maximum surface roughness no greater than 18 μm. However, 20 microinches translates into .508 μm, 10 microinches translates into .254 μm, and 5 microinches translates into .127 μm. Clearly, the claimed surface roughnesses are well below the 3 μm median surface roughness set by Tanaka et al., and they are not associated with a mounting area. Accordingly, Tanaka et al. fails to disclose any of these claimed surface roughnesses. Further, claim 6 recites that the at least one surface of the conductive circuit trace includes a surface parallel and proximal to the surface of the circuit board or a surface perpendicular to the surface of the circuit board. Tanaka et al. fails to disclose polishing either of these claimed surfaces.

In view of the foregoing, it is respectfully submitted that Tanaka et al. fails to disclose, or even suggest, the elements of claims 1-6, 19, and 20. Accordingly, it is respectfully submitted that claims 1-6, 19, and 20 of the present application are not anticipated by Tanaka et al., and thus the Examiner has failed in his duty to establish at least a prima facie case of anticipation against claims 1-6, 19, and 20 of the present application. Therefore, it is respectfully requested that the anticipation rejection of claims 1-6, 19, and 20 be withdrawn.

CONCLUSION

In view of the foregoing, it is respectfully submitted that the Examiner has failed to establish a prima facie case of anticipation against the appealed claims. Thus, it is respectfully submitted that the final rejection of claims 1-6, 19, and 20 is improper and the reversal of same is clearly in order and respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 50-0206, and please credit any excess fees to such deposit account.

Respectfully submitted,

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